USB PD and Other Multi-fast Charging Protocol Chip CH235

USB PD Fast Charging Protocol Chip CH231

Datasheet

Version: 1C

https://wch-ic.com

1. Overview

CH235S is a Type-C single-port fast charging protocol chip in ESSOP-10 package, which supports Type-C fast charging protocols such as PD3.0/2.0 and PPS, and also supports Type-A fast charging protocols such as BC1.2. CH235S supports all kinds of voltage references such as TL431 or FB current regulation of DC-DC system, integrates VBUS detection and discharge functions, and provides undervoltage, overcurrent and overtemperature protection functions.

CH231K is a streamlined version of the CH235S, using the SOT23-6L package and omitting the DP/DM related Type-A protocol support, VBUS discharge function, current compensation and protection function, and overtemperature protection function.

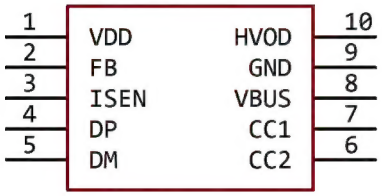
2. Features

- Support 3.3V-12.5V wide voltage input
- Support PD2.0/3.0, PPS, BC1.2 and other fast charging protocols.
- Support FB irrigation current regulation of TL431 and DC-DC devices with 20mV regulation accuracy.
- Support 100mV/1A cable compensation
- Built-in overcurrent protection OCP, overtemperature protection OTP, power overvoltage protection OVP, undervoltage protection UVP

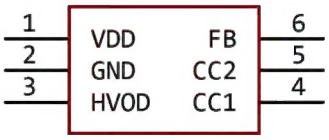
3. Applications

- AC Power Adapter
- Car Charger
- UPS
- Mobile Power

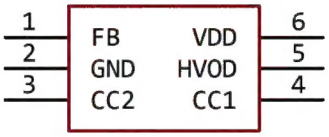
4. Package



CH235S (ESSOP-10)



CH231K (SOT23-6L)



CH231A (SOT23-6L)

5. Pin

Pin No.		Pin name	Pin description
CH235S	CH231K		
1	1	VDD	Internal power regulator voltage pin, connect a series resistor to the high voltage power supply, and connect a 1uF decoupling capacitor
9	2	GND	Common ground terminal
2	6	FB	Adjustable current sink input for voltage feedback regulation
10	3	HVOD	Power path PMOS control pin, requires external pull-up
7	4	CC1	Type-C PD fast charging protocol communication bus
6	5	CC2	
4	None	DP	Type-A fast charging protocol communication bus (Only CH235S)
5		DM	
8		VBUS	VBUS detection and discharge pin (Only CH235S)
3		ISEN	Current detection pin (Only CH235S)
0		E-PAD	EPAD, internally shorted to GND, welding is recommended. (Only CH235S)

6. Typical Application Circuit

Figure 6-1 CH231K reference circuit

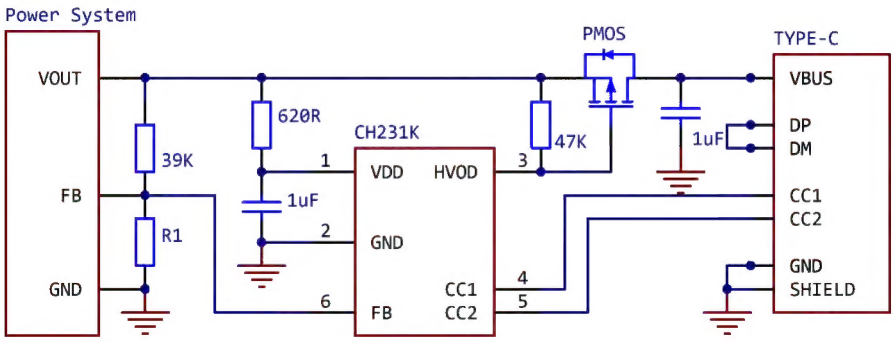
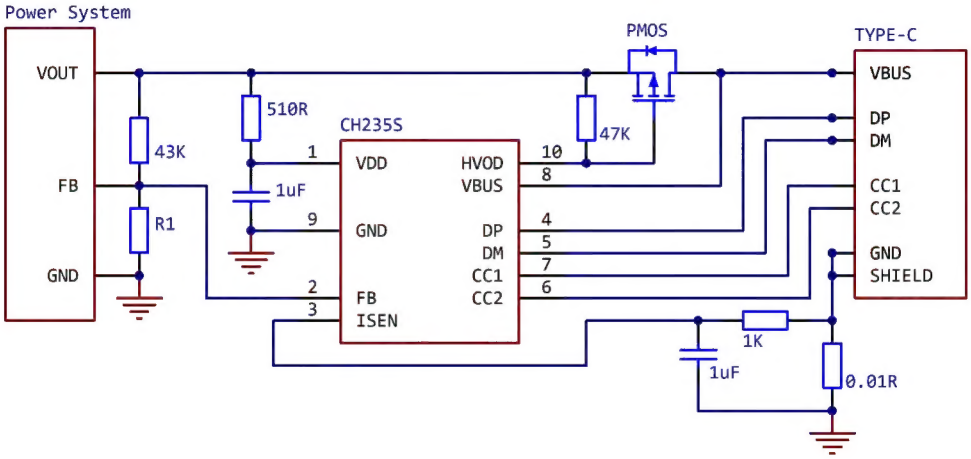


Figure 6-2 CH235S reference circuit



7. Function Description

7.1 VDD Pin

The VDD pin of CH235S/CH231K has a series regulator integrated inside. When using it, you need to connect a series resistor to the positive pole of the power output and connect a 1uF decoupling capacitor to GND. The recommended series resistor is 510R when using CH235S, and 620R when using CH231K. Appropriately reducing the resistance can improve the stability at low voltage, and increasing the resistance can reduce the static power consumption of the chip.

7.2 FB Pin

The FB pin of CH231K/CH231A/CH235S has a controllable current sink inside. It can control the output voltage of the power system by cooperating with the FB pin of a voltage reference such as TL431 or a DC-DC system. When using it, the upper bias resistor on the FB pin should be set to 39K (CH231K/CH231A) or 43K (CH235S), and the lower bias resistor should be calculated according to the FB voltage so that the default output voltage of the power system is 3.3V. The upper and lower bias resistors of the FB pin should use 1% or higher accuracy.

For CH231K/CH231A chip, take R1 resistance calculation in Figure 6.1 as an example:
For TL431 with FB voltage of 2.5V, the upper bias is 39K, the lower bias resistor R1 is 120K, and the default output voltage is:

$$((39/120)+1)*2.5 = 3.3125V$$

For DC-DC system with FB voltage of 0.8V, the upper bias is 39K, the lower bias resistor R1 is 12.5K, and the default output voltage is:

$$((39/12.5)+1)*0.8 = 3.296V$$

For CH235S chip, take R1 resistance calculation in Figure 6.2 as an example:
For TL431 with FB voltage of 2.5V, the upper bias is 43K, the lower bias resistor R1 is 130K, and the default output voltage is:

$$((43/130)+1)*2.5 = 3.3269V$$

For DC-DC system with FB voltage of 0.8V, the upper bias is 43K, the lower bias resistor R1 is 13.7K, and the default output voltage is:

$$((43/13.7)+1)*0.8 = 3.3109V$$

7.3 HVOD Pin

HVOD is an open-drain output pin, which is used to drive the power path PMOS and control the power output of VBUS. HVOD pin has no internal pull-up resistor and needs to be added externally.
When there is no device on the Type-C interface, the HVOD pin is in high impedance state, controlling the PMOS to shut down;
When there is a device in the Type-C interface, the HVOD pin outputs a low level to control the PMOS to turn on;
When overvoltage/overtemperature/overcurrent protection is detected, the HVOD pin will return to high impedance state, CH235S/CH231K will also reset and adjust the power path voltage back to 5V, disconnecting the VBUS

power supply to achieve protection.
If you do not want to use the power path PMOS, you can simply leave the HVOD pin floating.

7.4 CC1/CC2/DP/DM Pin

The CC1/CC2 pins are used for equipment access detection and PD protocol handshake, and the CH235S/CH231K supports the current broadcast of DFP mode 500mA, 1.5A or 3A defined by the Type-C protocol.
The DP/DM pin is used to shake hands with related protocols such as BC1.2, only for CH235S.

7.5 VBUS Pin

The VBUS pin is used to provide overvoltage protection and power supply discharge function, which can speed up the adjustment of power supply voltage and discharge the residual electricity of Type-C interface, only for CH235S.

7.6 ISEN Pin

The ISEN pin of CH235S is used to detect the charging current to realize the cable loss compensation function and overcurrent protection function during the charging process. The weak voltage on the sampling resistor is amplified by the 80x op amp inside the ISEN pin to realize the cable loss compensation function. For every 1A load current detected, the output voltage will be compensated by 0.1V.
At the same time, the voltage value after current sampling and amplification is also compared with the controllable DAC. If the result is higher than the maximum limiting current of the current protocol voltage level, the VBUS output is shut down to achieve the protection function.
ISEN pin and its related functions are only available on CH235S.

8. Parameters

8.1 Absolute Maximum Value (Critical or exceeding the absolute maximum value will probably cause the chip to work improperly or even be damaged)

Name	Parameter		Min.	Max.	Unit
TA	Ambient temperature during operation	VDD>3.2V	-40	105	℃
		VDD<3.0V	-40	85	℃
TS	Ambient temperature during storage		-55	125	℃
VDD	Operating power supply voltage (VDD pin connected to power supply, GND pin connected to ground)		-0.5	5.8	V
VIOCC	Voltage on non-high voltage pins CC1, CC2		-0.5	8	V
VIOUX	Voltage on non-high voltage pins DP, DM, FB and ISEN		-0.5	VDD+0.5	V
VIOHV	Voltage on high voltage pin HVOD, VBUS		-0.5	13.5	V
PD	The maximum power consumption of the entire chip (VDD voltage*current + VBUS discharge power consumption)			400	mW
ESD	Human body model (HBM)			2	KV

8.2 Electrical Parameters (Test condition: TA = 25℃)

Symbol	Parameter		Min.	Typ.	Max.	Unit
VDD	Working power supply voltage		3.0		3.6	V
VHV	Recommended high voltage range (HVOD, VBUS)		0	3~12	12.6	V
ICC6	Supply current during operation	CH235S		1.4	5	mA
		CH231K		0.8	2	
VLDO	Internal power regulator VDD parallel voltage regulator (3.3V gear)		3.24	3.3	3.36	V
ILDO	Internal power regulator VDD parallel sink current capability		0		30	mA
IFB	FB pin sink current			1~255		uA
IDVBUS3	Discharge current of CH235S VBUS pin at VDD=3.3V		7	10.5	15	mA
TOTA	Reference threshold temperature of CH235S over-temperature alarm module OTA			135±15		℃
VR	Power-on reset voltage threshold		2.2	2.4	2.6	V

9. Package Information

Package Form	Body Size	Pin Pitch		Order Model
ESSOP-10	3.9mm	1.00mm	39mil	CH235S
SOT23-6L	1.6mm	0.95mm	37mil	CH231K
SOT23-6L	1.6mm	0.95mm	37mil	CH231A

Note: The dimensioning unit is mm.

Figure 9-1 ESSOP-10 package

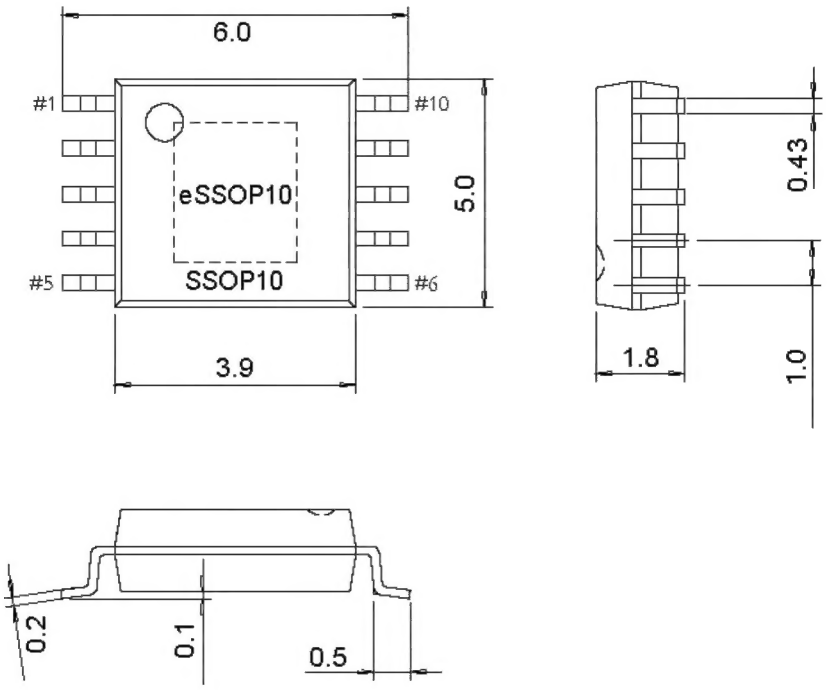
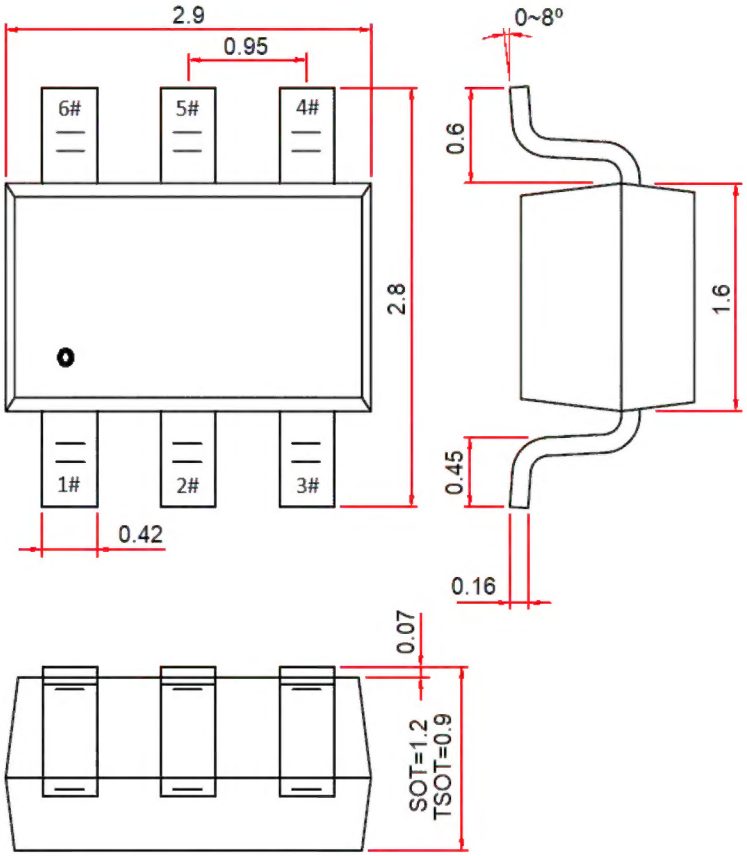



Figure 9-2 SOT23-6L package